INTEGRATED CONTROL OF POWER DELIVERY TO FIRING RESISTORS FOR INKJET PRINTHEAD ASSEMBLY

Cross-Reference to Related Applications

This Non-Provisional Patent Application is related to commonly assigned U.S. Patent Application Serial No. 09/253,411, filed on February 19, 1999, entitled "A HIGH PERFORMANCE PRINTING SYSTEM AND PROTOCOL," with Attorney Docket No. 10990391-1, and which is herein incorporated by reference.

The Field of the Invention

The present invention relates generally to inkjet printheads, and more particularly to controlling power delivery to firing resistors in inkjet printheads.

Background of the Invention

A conventional inkjet printing system includes a printhead, an ink supply which supplies liquid ink to the printhead, and an electronic controller which controls the printhead. The printhead ejects ink drops through a plurality of orifices or nozzles and toward a print medium, such as a sheet of paper, so as to print onto the print medium. Typically, the orifices are arranged in one or more arrays such that properly sequenced ejection of ink from the orifices causes characters or other images to be printed upon the print medium as the printhead and the print medium are moved relative to each other.

Typically, the printhead ejects the ink drops through the nozzles by rapidly heating a small volume of ink located in vaporization chambers with small electric heaters, such as thin film resisters. Heating the ink causes the ink to vaporize and be ejected from the nozzles. Typically, for one dot of ink, a remote printhead controller typically located as part of the processing electronics of a printer, controls activation of an electrical current from a power supply external to the printhead. The electrical current is passed through a selected thin

film resister to heat the ink in a corresponding selected vaporization chamber. The thin film resistors are herein referred to as firing resistors.

Typically, a high-current load on the power supply supplying the electrical current to the firing resistors occurs if a large number of firing resistors are simultaneously energized on a single printhead die. The resulting high electrical current flowing through parasitic resistances in conductors to the printhead die causes the voltage at the printhead die to sag. Less energy is delivered to the firing resistors as a result of this voltage sag at the printhead die.

In one conventional inkjet printing system, large by-pass capacitors are disposed adjacent to the printhead to alleviate a portion of this voltage sag. Nevertheless, any resistance between the large by-pass capacitors and the printhead is not compensated for in this conventional inkjet printing system. Furthermore, a DC sag on the power supply supplying the electrical current to the firing resistors under continuous load is also not compensated for in this conventional inkjet printing system.

In one conventional inkjet printing system, the duration of the power being supplied to the firing resistors is modulated in response to a change in the power supply voltage at the printhead. In this conventional inkjet printing system, constant energy is delivered to each firing resistor. Nevertheless, firing resistors receive more instantaneous power when only a few firing resistors are energized. The life of a firing resistor can be increased by reducing the amount of instantaneous power delivered to the firing resistor. Therefore, there is a desire to have both a fixed power applied to the firing resistors and a fixed duration that the fixed power is applied to the firing resistors.

For reasons stated above and for other reasons presented in greater detail in the Description of the Preferred Embodiments section of the present specification, an inkjet printhead is desired which minimizes instantaneous power delivered to firing resistors to thereby increase the life of the inkjet printhead.

Summary of the Invention

One aspect of the present invention provides an inkjet printhead including an internal power supply path, a power regulator providing an offset voltage from the internal power supply path voltage, and multiple primitives. Each primitive includes a group of nozzles, a corresponding group of firing resisters, and a corresponding group of switches. The switches are controllable to couple a selected firing resister of the group of firing resisters between the internal power supply path and the offset voltage to thereby permit electrical current to pass through the selected firing resister to cause a corresponding selected nozzle to fire.

In one embodiment, the power regulator is a linear power regulator. In one embodiment, the power regulator includes a digital-to-analog converter (DAC), such as a current-mode DAC, which is coupled to the internal power supply path. The DAC receives a digital offset command representing a desired offset voltage and provides an analog offset voltage from the internal power supply path voltage. In one embodiment, the power regulator includes a buffer amplifier that receives the analog offset voltage and provides a buffered offset voltage. In one embodiment, the power regulator includes multiple feedback amplifiers corresponding to the multiple primitives. Each feedback amplifier receives the buffered offset voltage and provides the offset voltage to a corresponding primitive.

In one embodiment, each switch includes a field effect transistor (FET).

In one embodiment, the printhead includes an internal power ground. Each feedback amplifier includes a first input coupled to the buffered offset voltage, a second input coupled to the offset voltage, and an output. The power regulator further includes multiple transistors. Each transistor is coupled between the internal power ground and the offset voltage and has a gate coupled to the output of a corresponding feedback amplifier. In one embodiment, each transistor is a FET.

In one embodiment, the printhead includes an internal power ground. Each feedback amplifier includes a first input coupled to the buffered offset voltage, a second input coupled to the offset voltage, and an output. Each firing

resister in a primitive includes a first terminal coupled to the internal power supply path and a second terminal. The group of switches in each primitive include subgroups of switches. Each subgroup of switches corresponds to a firing resister and includes a power transistor, a first switch, and a second switch. The power transistor is coupled between the second terminal of the firing resister and the internal power ground and has a control gate. The first switch is coupled between the drive line and the control gate of the power transistor. The second switch is coupled between the feedback line and the second terminal of the firing resistor. In one embodiment, the power transistor is a FET.

One aspect of the present invention provides an inkjet printhead assembly including at least one printhead. Each printhead includes an internal power supply path, a power regulator providing an offset voltage from the internal power supply path voltage, and multiple primitives. Each primitive includes a group of nozzles, a corresponding group of firing resisters, and a corresponding group of switches. The switches are controllable to couple a selected firing resister of the group of firing resisters between the internal power supply path and the offset voltage to thereby permit electrical current to pass through the selected firing resister to cause a corresponding selected nozzle to fire.

In one embodiment, the printhead assembly includes multiple printheads.

One aspect of the present invention provides an inkjet printing system including a first power supply and at least one printhead. Each printhead includes an internal power supply path coupled to the first power supply, a power regulator providing an offset voltage from the internal power supply path voltage, and multiple primitives. Each primitive includes a group of nozzles, a corresponding group of firing resisters, and a corresponding group of switches. The switches are controllable to couple a selected firing resister of the group of firing resisters between the internal power supply path and the offset voltage to thereby permit electrical current to pass through the selected firing resister to cause a corresponding selected nozzle to fire.

In one embodiment, the printhead includes a processor supplying the digital offset command. In another embodiment, the inkjet printing system

includes an electronic controller supplying the digital offset command to the printhead.

One aspect of the present invention provides a method of inkjet printing in an inkjet printhead. The method provides an internal power supply path and provides an offset voltage from the internal power supply path voltage. The method couples a selected firing resister of a group of firing resisters between the internal power supply path and the offset voltage to cause electrical current to pass through the selected firing resister to cause a corresponding selected nozzle to fire.

In one embodiment, the method includes converting a digital offset command representing a desired offset voltage to an analog offset voltage from the internal power supply path voltage. In one embodiment, the method includes buffering the analog offset voltage. In one embodiment, the method includes receiving the buffered analog offset voltage at a feedback amplifier, and providing the offset voltage with the feedback amplifier. In one embodiment, the method includes supplying the digital offset command.

The integrated control of power delivery to the firing resistors in the inkjet printhead according to the present invention permits a fixed applied power to the energized firing resistors and a fixed duration for which the applied power is applied to the energized firing resistors. The integrated control of power delivery to the firing resistors according to the present invention maintains a substantially constant amount of power delivered to the firing resistors, even when only a few firing resistors are energized at a given time. The reduced power variation increases the firing resistor life, which thereby yields a longer life for the printhead according to the present invention.

Brief Description of the Drawings

Figure 1 is a block diagram illustrating one embodiment of an inkjet printing system.

Figure 2 is an enlarged schematic cross-sectional view illustrating portions of one embodiment of a printhead die in the printing system of

Figure 1.

Figure 3 is a block diagram illustrating portions of one embodiment of an inkjet printhead having firing resistors grouped together into primitives.

Figure 4 is a block and schematic diagram illustrating portions of one embodiment of nozzle drive logic and circuitry employable in a primitive of an inkjet printhead.

Figure 5 is a block and schematic diagram illustrating portions of one embodiment of an inkjet printhead according to the present invention having integrated control of power delivery to firing resistors.

Figure 6 is a block and schematic diagram illustrating portions of another embodiment of an inkjet printhead according to the present invention having integrated control of power delivery to firing resistors.

Figure 7 is a block and schematic diagram illustrating portions of one embodiment of a primitive of the inkjet printhead of Figure 6.

Description of the Preferred Embodiments

In the following detailed description of the preferred embodiments, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific embodiments in which the invention may be practiced. In this regard, directional terminology, such as "top," "bottom," "front," "back," "leading," "trailing," etc., is used with reference to the orientation of the Figure(s) being described. The inkjet printhead assembly and related components of the present invention can be positioned in a number of different orientations. As such, the directional terminology is used for purposes of illustration and is in no way limiting. It is to be understood that other embodiments may be utilized and structural or logical changes may be made without departing from the scope of the present invention. The following detailed description, therefore, is not to be taken in a limiting sense, and the scope of the present invention is defined by the appended claims.

Figure 1 illustrates one embodiment of an inkjet printing system 10. Inkjet printing system 10 includes an inkjet printhead assembly 12, an ink supply assembly 14, a mounting assembly 16, a media transport assembly 18, and an

electronic controller 20. At least one power supply 22 provides power to the various electrical components of inkjet printing system 10. Inkjet printhead assembly 12 includes at least one printhead or printhead die 40 which ejects drops of ink through a plurality of orifices or nozzles 13 and toward a print medium 19 so as to print onto print medium 19. Print medium 19 is any type of suitable sheet material, such as paper, card stock, transparencies, Mylar, and the like. Typically, nozzles 13 are arranged in one or more columns or arrays such that properly sequenced ejection of ink from nozzles 13 causes characters, symbols, and/or other graphics or images to be printed upon print medium 19 as inkjet printhead assembly 12 and print medium 19 are moved relative to each other.

Ink supply assembly 14 supplies ink to printhead assembly 12 and includes a reservoir 15 for storing ink. As such, ink flows from reservoir 15 to inkjet printhead assembly 12. Ink supply assembly 14 and inkjet printhead assembly 12 can form either a one-way ink delivery system or a recirculating ink delivery system. In a one-way ink delivery system, substantially all of the ink supplied to inkjet printhead assembly 12 is consumed during printing. In a recirculating ink delivery system, however, only a portion of the ink supplied to printhead assembly 12 is consumed during printing. As such, ink not consumed during printing is returned to ink supply assembly 14.

In one embodiment, inkjet printhead assembly 12 and ink supply assembly 14 are housed together in an inkjet cartridge or pen. In another embodiment, ink supply assembly 14 is separate from inkjet printhead assembly 12 and supplies ink to inkjet printhead assembly 12 through an interface connection, such as a supply tube. In either embodiment, reservoir 15 of ink supply assembly 14 may be removed, replaced, and/or refilled. In one embodiment, where inkjet printhead assembly 12 and ink supply assembly 14 are housed together in an inkjet cartridge, reservoir 15 includes a local reservoir located within the cartridge as well as a larger reservoir located separately from the cartridge. As such, the separate, larger reservoir serves to refill the local reservoir. Accordingly, the separate, larger reservoir and/or the local reservoir may be removed, replaced, and/or refilled.

Mounting assembly 16 positions inkjet printhead assembly 12 relative to media transport assembly 18 and media transport assembly 18 positions print medium 19 relative to inkjet printhead assembly 12. Thus, a print zone 17 is defined adjacent to nozzles 13 in an area between inkjet printhead assembly 12 and print medium 19. In one embodiment, inkjet printhead assembly 12 is a scanning type printhead assembly. As such, mounting assembly 16 includes a carriage for moving inkjet printhead assembly 12 relative to media transport assembly 18 to scan print medium 19. In another embodiment, inkjet printhead assembly 12 is a non-scanning type printhead assembly. As such, mounting assembly 16 fixes inkjet printhead assembly 12 at a prescribed position relative to media transport assembly 18. Thus, media transport assembly 18 positions print medium 19 relative to inkjet printhead assembly 12.

Electronic controller or printer controller 20 typically includes a processor, firmware, and other printer electronics for communicating with and controlling inkjet printhead assembly 12, mounting assembly 16, and media transport assembly 18. Electronic controller 20 receives data 21 from a host system, such as a computer, and includes memory for temporarily storing data 21. Typically, data 21 is sent to inkjet printing system 10 along an electronic, infrared, optical, or other information transfer path. Data 21 represents, for example, a document and/or file to be printed. As such, data 21 forms a print job for inkjet printing system 10 and includes one or more print job commands and/or command parameters.

In one embodiment, electronic controller 20 controls inkjet printhead assembly 12 for ejection of ink drops from nozzles 13. As such, electronic controller 20 defines a pattern of ejected ink drops which form characters, symbols, and/or other graphics or images on print medium 19. The pattern of ejected ink drops is determined by the print job commands and/or command parameters.

In one embodiment, inkjet printhead assembly 12 includes one printhead 40. In another embodiment, inkjet printhead assembly 12 is a wide-array or multi-head printhead assembly. In one wide-array embodiment, inkjet printhead assembly 12 includes a carrier, which carries printhead dies 40, provides

electrical communication between printhead dies 40 and electronic controller 20, and provides fluidic communication between printhead dies 40 and ink supply assembly 14.

A portion of one embodiment of a printhead die 40 is illustrated schematically in Figure 2. Printhead die 40 includes an array of printing or drop ejecting elements 42. Printing elements 42 are formed on a substrate 44 which has an ink feed slot 441 formed therein. As such, ink feed slot 441 provides a supply of liquid ink to printing elements 42. Each printing element 42 includes a thin-film structure 46, an orifice layer 47, and a firing resistor 48. Thin-film structure 46 has an ink feed channel 461 formed therein which communicates with ink feed slot 441 of substrate 44. Orifice layer 47 has a front face 471 and a nozzle opening 472 formed in front face 471. Orifice layer 47 also has a nozzle chamber 473 formed therein which communicates with nozzle opening 472 and ink feed channel 461 of thin-film structure 46. Firing resistor 48 is positioned within nozzle chamber 473 and includes leads 481 which electrically couple firing resistor 48 to a drive signal and ground.

During printing, ink flows from ink feed slot 441 to nozzle chamber 473 via ink feed channel 461. Nozzle opening 472 is operatively associated with firing resistor 48 such that droplets of ink within nozzle chamber 473 are ejected through nozzle opening 472 (e.g., normal to the plane of firing resistor 48) and toward a print medium upon energization of firing resistor 48.

Example embodiments of printhead dies 40 include a thermal printhead, a piezoelectric printhead, a flex-tensional printhead, or any other type of inkjet ejection device known in the art. In one embodiment, printhead dies 40 are fully integrated thermal inkjet printheads. As such, substrate 44 is formed, for example, of silicon, glass, or a stable polymer and thin-film structure 46 is formed by one or more passivation or insulation layers of silicon dioxide, silicon carbide, silicon nitride, tantalum, poly-silicon glass, or other suitable material. Thin-film structure 46 also includes a conductive layer which defines firing resistor 48 and leads 481. The conductive layer is formed, for example, by aluminum, gold, tantalum, tantalum-aluminum, or other metal or metal alloy.

Printhead assembly 12 can include any suitable number (N) of printheads 40, where N is at least one. Before a print operation can be performed, data must be sent to printhead 40. Data includes, for example, print data and non-print data for printhead 40. Print data includes, for example, nozzle data containing pixel information, such as bitmap print data. Non-print data includes, for example, command/status (CS) data, clock data, and/or synchronization data. Status data of CS data includes, for example, printhead temperature or position, printhead resolution, and/or error notification.

One embodiment of printhead 40 is illustrated generally in block diagram form in Figure 3. Printhead 40 includes multiple firing resistors 48 which are grouped together into primitives 50. As illustrated in Figure 3, printhead 40 includes N primitives 50. The number of firing resistors 48 grouped in a given primitive can vary from primitive to primitive or can be the same for each primitive in printhead 40. Each firing resistor 48 has an associated switching device 52, such as a field effect transistor (FET). A single power lead provides power to the source or drain of each FET 52 for each resistor in each primitive 50. Each FET 52 in a primitive 50 is controlled with a separately energizable address lead coupled to the gate of the FET 52. Each address lead is shared by multiple primitives 50. As described in detail below, the address leads are controlled so that only one FET 52 is switched on at a given time so that only a single firing resistor 48 has electrical current passed through it to heat the ink in a corresponding selected vaporization chamber at the given time.

In the embodiment illustrated in Figure 3, primitives 50 are arranged in printhead 40 in two columns of N/2 primitives per column. Other embodiments of printhead 40, however, have primitives arranged in many other suitable arrangements.

Portions of one embodiment of nozzle drive logic and circuitry 60 of a primitive 50 are generally illustrated in block and schematic diagram form in Figure 4. The portions illustrated in Figure 4 represent the main logic and circuity for implementing the nozzle firing operation of nozzle drive logic and circuity 60. However, practical implementations of nozzle drive logic and

circuitry 60 can include various other complex logic and circuitry not illustrated in Figure 4.

Nozzle drive logic and circuitry 60 receives nozzle data on a path 64, a nozzle address on a path 66, and a fire pulse on a path 68. Nozzle drive logic and circuitry 60 also receives primitive power on a power line 70 and primitive ground on a ground line 72. Nozzle drive logic and circuitry 60 combines the nozzle data on path 64, the nozzle address on path 66, and the fire pulse on path 68 to sequentially switch electrical current from primitive power line 70 through firing resistors 48 to ground line 72. The nozzle data on path 64 represents the characters, symbols, and/or other graphics or images to be printed. The nozzle address on path 66 controls the sequence of which nozzle is to be fired at a given time (i.e., the nozzle firing order). The nozzle address on path 66 is cycled through so that all nozzles can be fired, but only a single firing resistor 48 in primitive 50 is operated at a given time. The fire pulse on path 68 controls the timing of the activation of the electrical current from a power supply external to the printhead, such as power supply 22 (shown in Figure 1).

In the embodiment of nozzle drive logic and circuitry 60 illustrated in Figure 4, the nozzle address provided on path 66 is an encoded address. Thus, the nozzle address on path 66 is provided to N address decoders 82a, 82b, ..., 82n. In this embodiment, the nozzle address on path 66 can represent one of N addresses representing one of N nozzles in the primitive 50. Accordingly, the address decoders 82 respectively provide an active output signal if the nozzle address on path 66 represents the nozzle associated with a given address decoder.

Nozzle drive logic and circuitry 60 includes AND gates 84a, 84b, ..., 84n, which receive the N outputs from the address decoders 82a-82n. AND gates 84a-84n also respectively receive corresponding ones of the N nozzle data bits from path 64. AND gates 84a-84n also each receive the fire pulse provided on path 68. The outputs of AND gates 84a-84n are respectively coupled to corresponding control gates of FETs 52a-52n. Thus, for each AND gate 84, if the corresponding nozzle 13 has been selected to receive data based on the nozzle data input bit from path 64, the fire pulse on line 68 is active, and the

nozzle address on line 66 matches the address of the corresponding nozzle, the AND gate 84 activates its output which is coupled to the control gate of a corresponding FET 52.

Each FET 52 has its source coupled to primitive ground line 72 and its drain coupled to a corresponding firing resistor 48. Firing resistors 48a-48n are respectively coupled between primitive power line 70 and the drains of corresponding FETs 52a-52n.

Thus, when the combination of the nozzle data bit, the decoded address bit, and the fire pulse provide three active inputs to a given AND gate 84, the given AND gate 84 provides an active pulse to the control gate of the corresponding FET 52 to thereby turn on the corresponding FET 52 which correspondingly causes current to be passed from primitive power line 70 through the selected firing resistor 48 to primitive ground line 72. The electrical current being passed through the selected firing resistor 48 heats the ink in a corresponding selected vaporization chamber to cause the ink to vaporize and be ejected from the corresponding nozzle 13.

One embodiment of a printhead 40 having a linear power regulator 100 according to the present invention is illustrated generally in block and schematic diagram form in Figure 5. Printhead 40 employs linear power regulator 100 to compensate for off-printhead die parasitic resistances which cause the power supply voltage (Vpp) to sag at the input to printhead 40. Printhead 40 receives Vpp power from power supply 22 at Vpp input pin(s) 90 and receives a corresponding power ground at input pin(s) 94. An internal Vpp power supply path 92 is coupled to Vpp power pins 90 to internally supply Vpp power to the firing resistors 48 in printhead 40. An internal power ground 96 is coupled to power ground pins 94 to internally supply the corresponding power ground to the firing resistors 48 in printhead 40.

Each of the primitives 50a-50n includes a corresponding one of the primitive power lines 70a-70n which is directly coupled to the internal Vpp power supply path 92. Each of the primitives 50a-50n includes a corresponding one of the primitive ground lines 72a-72n which is not directly coupled to the

internal power ground 96. Rather, primitive ground lines 72a-72n are controlled with linear power regulator 100 according to the present invention.

Linear power regulator 100 includes a current-mode digital-to-analog converter (DAC) 102, a buffer amplifier 104, and a series of feedback amplifiers 106a, 106b,...,106n. Each of the feedback amplifiers 106a-106n corresponds to a corresponding one of the primitives 50a-50n, where each primitive 50 can only have one firing resistor 48 energized at a given time.

DAC 102 receives a digital offset command on lines 108. The internal Vpp power supply path 92 is coupled to DAC 102 and provides a reference voltage for DAC 102. DAC 102 is programmed by the digital offset command on lines 108 to produce an analog offset voltage from the internal Vpp power supply path 92 voltage to thereby track any movement of the Vpp power supply at the Vpp input pins 90 of printhead 40. The digital offset command on lines 108 represents the amount of offset voltage necessary to compensate for off-printhead die parasitic resistances that cause the Vpp power supply voltage to sag at the input to printhead 40.

In one embodiment, printhead 40 includes a processor 98 which provides the digital offset command on lines 108. In another embodiment, the digital offset command is provided by electronic controller 20 to printhead 40. In yet another embodiment, the digital offset command on lines 108 is provided by a processor external to the printhead(s) 40 but contained within printhead assembly 12. In any of these embodiments, the digital offset command is typically stored in a register which is read and written by a processor, such as processor 98, via an internal bus of printhead 40.

DAC 102 coverts the digital offset command on lines 108 to the analog offset voltage from the internal Vpp power supply path voltage and provides the analog offset voltage on line 110. The analog offset voltage provided on line 110 is coupled to the positive input of buffer amplifier 104. Buffer amplifier 104 has a unity gain and provides a buffered offset voltage on a line 114 having a low-impedance output characteristic so that the offset voltage on line 114 can be distributed across the printhead die 40. The offset voltage on line 114 is fed back to the negative input of buffer amplifier 104.

The offset voltage on line 114 is provided to the negative input terminal of each feedback amplifier 106a-106n. The positive input of each feedback amplifier 106a-106n is respectively coupled to a corresponding one of the primitive ground lines 72a-72n. The output of each feedback amplifier 106a-106n is respectively coupled to the gate of a corresponding FET 116a, 116b,...,116n.

The source of each FET 116a-116n is coupled to internal power ground 96. The drain of each FET 116a-116n is respectively coupled to a corresponding one of the primitive ground lines 72a-72n. The feedback configuration between each FET 116 and feedback amplifier 106 forces the buffered offset voltage on line 114 to the respective primitive ground line 72.

Only one resistor 48 inside of each primitive 50 can be energized at a given time. An energized firing resistor 48 in a given primitive 50 has the offset voltage coupled to its low-side instead of the internal power ground 96 and the internal Vpp power supply path 92 coupled to its high-side. Since the high-side of the energized firing resistor 48 is coupled to the internal Vpp power supply path 92, the energized firing resistor 48 has a constant voltage across it equal to a difference of the Vpp voltage and the programmed offset voltage even if the Vpp voltage sags. This tracking of Vpp voltage movement results in a substantially constant power being delivered to the energized firing resistors 48 in printhead 40.

An alternative embodiment of a printhead 240 having a linear power regulator 200 according to the present invention is illustrated generally in block and schematic diagram form in Figure 6. Printhead 240 employs linear power regulator 200 to compensate for off-printhead die parasitic resistances which cause the power supply voltage (Vpp) to sag at the input to printhead 240. Printhead 240 receives Vpp power from power supply 22 at Vpp input pin(s) 290 and receives a corresponding power ground at input pin(s) 294. An internal Vpp power supply path 292 is coupled to Vpp power pins 290 to internally supply Vpp power to the firing resistors 248 (shown in Figure 7) in printhead 240. An internal power ground 296 is coupled to power ground pins 294 to

internally supply the corresponding power ground to the firing resistors 248 in printhead 240.

Each of N primitives 250a, 250b,...,250n includes a corresponding one of primitive power lines 270a, 270b,...,270n which is directly coupled to the internal Vpp power supply path 292. Each of the primitives 250a-250n includes a corresponding one of primitive ground lines 272a, 272b,...,272n which is directly coupled to the internal power ground 296.

Linear power regulator 200 includes a current-mode digital-to-analog converter (DAC) 202, a buffer amplifier 204, and a series of feedback amplifiers 206a, 206b,...,206n. Each of the feedback amplifiers 206a-206n corresponds to a corresponding one of the primitives 250a-250n, where each primitive 250 can only have one firing resistor 248 energized at a given time.

DAC 202 receives a digital offset command on lines 208. The internal Vpp power supply path 292 is coupled to DAC 202 and provides a reference voltage for DAC 202. DAC 202 is programmed by the digital offset command on lines 208 to produce an analog offset voltage from the internal Vpp power supply path 292 voltage to thereby track any movement of the Vpp power supply at the Vpp input pins 290 of printhead 240. The digital offset command on lines 208 represents the amount of offset voltage necessary to compensate for off-printhead die parasitic resistances that cause the Vpp power supply voltage to sag at the input to printhead 240.

In one embodiment, printhead 240 includes a processor 298 which provides the digital offset command on lines 208. In another embodiment, the digital offset command is provided by electronic controller 20 to printhead 240. In yet another embodiment, the digital offset command on lines 208 is provided by a processor external to the printhead(s) 240 but contained within printhead assembly 12. In any of these embodiments, the digital offset command is typically stored in a register which is read and written by a processor, such as processor 298, via an internal bus of printhead 240.

DAC 202 coverts the digital offset command on lines 208 to the analog offset voltage from the internal Vpp power supply path voltage and provides the analog offset voltage on line 210. The analog offset voltage provided on line

210 is coupled to the positive input of buffer amplifier 204. Buffer amplifier 204 has a unity gain and provides a buffered offset voltage on a line 214 having a low-impedance output characteristic so that the offset voltage on line 214 can be distributed across the printhead die 240. The offset voltage on line 214 is fed back to the negative input of buffer amplifier 204.

The offset voltage on line 214 is provided to the negative input terminal of each feedback amplifier 206a-206n. The positive input of each feedback amplifier 206a-206n is respectively coupled to a corresponding one of feedback lines 218a, 218b,...,218n of primitives 250a-250n. The output of each feedback amplifier 206a-206n is respectively coupled to a corresponding one of FET drive lines 216a, 216b,...,218n of primitives 250a-250n.

Portions of one embodiment of a primitive 250 of printhead 240 are generally illustrated in block and schematic diagram form in Figure 7. Primitive 250 includes N firing resistors 248a, 248b,...,248n. Each firing resistor 248 has a first terminal coupled to primitive power line 270. Primitive 250 includes N power FETs 252a, 252b,...,252n. Each power FET 252 has its source coupled to primitive ground line 272 and its drain coupled to a second terminal of a corresponding firing resistor 248.

A digital nozzle firing controller 220 has N outputs for controlling N pairs of analog switches (223a, 224a), (223b, 224b),...,(223n, 224n). In addition, nozzle firing controller 220 has an off output, which when activated controls a switch 222 to disable all firing resistors 248 in primitive 250. The N other outputs of nozzle firing controller 220 are operated with a digital state machine or other suitable logic so that at most only one of the N outputs are active at a given time so that at most only one switch pair (223, 224) is switched on at a given time. Switches 222, 223, and 224 can be implemented with low-impedance non-power FETs.

Each switch 223 is coupled between a control gate of a corresponding power FET 252 and the FET drive line 216 provided as the output of feedback amplifier 206. Each switch 224 is coupled between the second terminal of a corresponding firing resistor 248 and the feedback line 218 provided to the positive input of feedback amplifier 206.

Thus, in operation, when nozzle firing controller 220 selects a switch pair (223, 224) to be turned on, the FET drive line 216 is coupled to the control gate of the corresponding selected power FET 252 and the feedback line 218 is coupled to the second terminal of the corresponding selected firing resistor 248 and to the drain of the selected power FET 252. This feedback configuration between the selected power FET 252 and feedback amplifier 206 provides the offset voltage 214 on feedback line 218 to the second terminal of the selected firing resistor 248. Since, the selected firing resistor 248 also has the primitive power line coupled to its first input, the selected firing resistor is energized and electrical current is passed through the firing resistor to heat the ink in a corresponding selected vaporization chamber.

Only one resistor 248 inside of each primitive 250 can be energized at a given time. An energized firing resistor 248 in a given primitive 250 has the offset voltage coupled to its low-side instead of the internal power ground 296 and the internal Vpp power supply path 292 coupled to its high-side. Since the high-side of the energized firing resistor 248 is coupled to the internal Vpp power supply path 292, the energized firing resistor 248 has a constant voltage across it equal to a difference of the Vpp voltage and the programmed offset voltage even if the Vpp voltage sags. This tracking of Vpp voltage movement results in a substantially constant power being delivered to the energized firing resistors 248 in printhead 240.

The linear power regulator 100/200 of printhead 40/240 according to the present invention permits a fixed applied power to the energized firing resistors 48/248 and a fixed duration for which the applied power is applied to the energized firing resistors 48/248. In this way, the amount of power delivered to the firing resistors is kept to at a substantially constant level , even when only a few firing resistors are energized at a given time. The reduced power variation increases the firing resistor life, which thereby yields a longer life for the printhead 40/240 according to the present invention.

Although specific embodiments have been illustrated and described herein for purposes of description of the preferred embodiment, it will be appreciated by those of ordinary skill in the art that a wide variety of alternate

and/or equivalent implementations calculated to achieve the same purposes may be substituted for the specific embodiments shown and described without departing from the scope of the present invention. Those with skill in the chemical, mechanical, electro-mechanical, electrical, and computer arts will readily appreciate that the present invention may be implemented in a very wide variety of embodiments. This application is intended to cover any adaptations or variations of the preferred embodiments discussed herein. Therefore, it is manifestly intended that this invention be limited only by the claims and the equivalents thereof.